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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,788	12/26/2001	Akihisa Nakamura	016907-1347	5875
22428	7590	05/04/2005	EXAMINER	
FOLEY AND LARDNER SUITE 500 3000 K STREET NW WASHINGTON, DC 20007			PHAM, CHRYSTINE	
			ART UNIT	PAPER NUMBER
			2192	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/025,788

Applicant(s)

NAKAMURA, AKIHISA

Examiner

Chrystine Pham

Art Unit

2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 April 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/26/2001.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to paper filed on January 13th 2005.

Election/Restrictions

2. Applicant's election without traverse of Group I, claims 1-6, in the reply filed on January 13th 2005, is acknowledged. Claim 7 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on January 13th 2005.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "RTL description data in the entity portion" in lines 4-5.

There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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6. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Sharma et al. (Sharma et al., US 5841663).

Claim 1

Sharma et al. teach a method of generating an ASIC (see at least *ASIC designs* col.1:64-col.2:50)

design database (see at least *parameterized HDL library modules* col.1:64-col.2:50), comprising:

- o extracting, when a function design using description data comprising a header portion (see at least *parameterized HDL module, entity description* col.1:64-col.2:14; *HDL description, element, properties, medium speed, area, power consumptions* col.11:55-col.12:52) and an entity portion has been performed (see at least *parameterized HDL module, behavioral description, function* col.1:64-col.2:14; *behavioral description* col.20:1-56; *behavioral description* 23:1-67), information necessary for reuse design (see at least *parameter values* col.2:15-50; *HDL description, element, properties, medium speed, area, power consumptions* col.11:55-col.12:52; *layout area, port width values* col.14:28-37) from various execution results of the entity portion (see at least *simulated, netlist implementations, parameter values* col.2:15-50; *datapath instances* col.15:19-50; *implementations, parameterized HDL module* col.26:48-60);
- o writing the extracted information necessary for reuse design in the header portion of the description data (see at least *entity description, parameters, parameter values* col.2:1-50; *HDL description, element, properties, medium speed, area, power consumptions* col.11:55-col.12:52; *layout area, port width values* col.14:28-37; *rt1dplnstOperClass, long real area, layout area* col.15:60-col.16:45; *circuit area, power consumption* col.17:65-col.18:10; *entity description, parameters, input ports, output ports, bit width* col.19:34-67; *entity description, parameter* col.20:1-30; *entity description, parameter "N", parameter "M"* col.23:1-67); and
- o storing, as one file at a predetermined location, the description data comprising the header portion in which the information necessary for reuse is written, and the entity portion (see at least *parameterized HDL module, parameterized HDL library modules* col.1:64-col.2:50; 300 FIG.16 & associated text).

Claim 2

The rejection of base claim 1 is incorporated. Sharma et al. further teach wherein the information necessary for reuse, which is extracted from the various execution results of the entity portion, is at least a simulation time, layout area, timing, and power consumption (see at least *HDL description, element, properties, medium speed, area, power consumptions* col.11:55-col.12:52; *layout area, port width values* col.14:28-37; *entity description, parameters, input ports, output ports, bit width* col.19:34-67).

Claim 3

The rejection of base claim 1 is incorporated. Sharma et al. further teach wherein the entity portion of said description data is described using a hardware description language (see at least *HDL language* col.1:64-col.2:50; *HDL description, element* col.11:54-col.12:52; *behavior, circuit element, HDL* col.18:52-67).

Claim 4

The rejection of base claim 1 is incorporated. Sharma et al. further teach wherein the entity portion of said description data is RTL description data described in a register transfer level (see at least *RTL description, elements* col.12:40-52; *RTL description 34, parser 32* FIG.16 & associated text).

Claim 5

The rejection of base claim 1 is incorporated. Sharma et al. further teach wherein in the file stored at the predetermined location, information written in the header portion and RTL description data in the entity portion (see at least *RTL description, elements* col.12:40-52; *RTL description 34, parser 32* FIG.16 & associated text) are uniformly managed (see at least *parameterized HDL module parameterized HDL library modules* col.1:64-col.2:50; 300 FIG.16 & associated text).

Claim 6

Sharma et al. teach a method of generating an ASIC design database, comprising:

- extracting, when a function design using RTL description data (see at least *RTL description, elements* col.12:40-52; *RTL description 34, parser 32* FIG.16 & associated text) comprising a header portion (see at least *parameterized HDL module, entity description* col.1:64-col.2:14; *HDL description, element, properties, medium speed, area, power consumptions* col.11:55-col.12:52) and an entity portion and made in a register transfer level has been performed (see at least *parameterized HDL module, behavioral description, function* col.1:64-col.2:14; *behavioral description* col.20:1-56; *behavioral description 23:1-67*), information necessary for reuse design (see at least *parameter values* col.2:15-50; *HDL description, element, properties, medium speed, area, power consumptions* col.11:55-col.12:52; *layout area, port width values* col.14:28-37) from various execution results of the entity portion (see at least *simulated, netlist implementations, parameter values* col.2:15-50; *datapath instances* col.15:19-50; *implementations, parameterized HDL module* col.26:48-60);
- writing the extracted information necessary for reuse design in the header portion of the RTL description data (see at least *entity description, parameters, parameter values* col.2:1-50; *HDL description, element, properties, medium speed, area, power consumptions* col.11:55-col.12:52; *layout area, port width values* col.14:28-37; *rt1dpInstOperClass, long real area, layout area* col.15:60-col.16:45; *circuit area, power consumption* col.17:65-col.18:10; *entity description, parameters, input ports, output ports, bit width* col.19:34-67; *entity description, parameter* col.20:1-30; *entity description, parameter "N", parameter "M"* col.23:1-67); and
- storing, as one file at a predetermined location, the RTL description data comprising the header portion in which the information necessary for reuse is written, and the entity portion (see at least *parameterized HDL module, parameterized HDL library modules* col.1:64-col.2:50; 300 FIG.16 & associated text).


Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chrystine Pham whose telephone number is 571-272-3702. The examiner can normally be reached on Mon-Fri, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CP
April 29, 2005


TUAN DAM
SUPERVISORY PATENT EXAMINER